On the origin of gate oscillation of Power devices

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As power devices, especially for superjunction MOSFETs and SiC MOSFETs, are scaled down to smaller dimensions, the gate ringing becomes more prominent in dynamic switching. The exact origin of power devices' gate ringing has not been so far identified as the conventional three-terminal measurement method cannot capture the dynamic behavior of the device, in particular the redistribution of charge between the different internal capacitive components in the power devices' structure. In this presentation, it is found that, during the di/dt period, the gate ringing is initially triggered by the parasitic source inductance and this leads to a potential shift of both the gate and the source potential. The shifted gate poential will result in the the rapid currrent change across the gate reistor and the parasitic gate inductance. Finally, the rapid change in the gate current produces a gate oscillation with the parasitic gate inductance and the gate capacitance. Figure 1 shows the simulated gate oscillation phenomenon during the inductive switching of a SiC MOSFET.

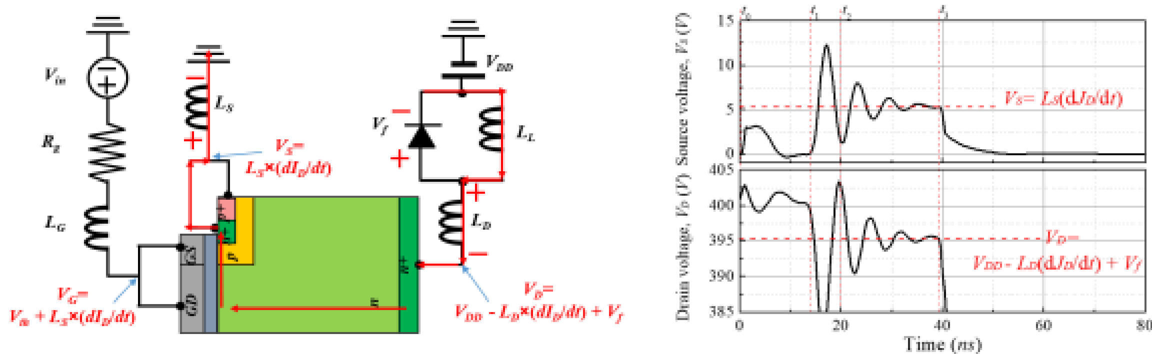

Fig. 1. The configuration of the inductive switching system with parasitic inductances and the waveforms of the source and the drain voltage

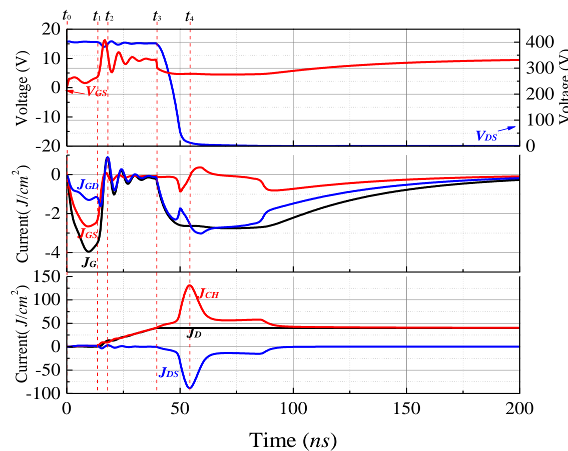

Fig. 2. The simulated waveforms of gate oscillations with 5-contacts method.

References

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