Patterning and metrology challenges in EUV lithography

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As semiconductor industry continues its push for device scaling, fabrication processes become more complex. The introduction of EUV lithograhy has allowed for simplification in process integration schemes compared with immersion mulitpatterning, but as device shrink continues and new device architectures are introduced, important patterning and metrology challenges remain.

Variability control is key, so that the Edge Placement Error (EPE) and defectivity can be kept within the targets of the corresponding node, therefore optical inspection and massive e-beam metrology is needed to characterize this variability.

The near future introduction of high NA EUV systems will allow to continue the device scaling roadmap, but associated challenges appear for patterning and metrology such as use of thin resists, depth of focus, SEM contrast... Machine learning methods can be used to enhance the signal to noise ratio and provide more accurate and faster measurements as well as defect defection in non-regular logic and memory structures.

Besides traditional pitch scaling, the introduction of 3D device architectures such as CFET and 3D processes like bonding, backside power delivery, 3D DRAM, poses new challenges for patterning and metrology besides the traditional top view inspection, as new and failure mechanisms must be understood.

In this paper we will discuss imec research on EUV patterning and metrology to address these challenges and enable next generation devices.