Dr. Changhyun Cho

(Ex. SK hynix & Samsung Electronics, Korea)

Changhyun Cho is expert of process integration expert in memory device. He has more than 35 patents and 20 papers. In 1995, he joined Samsung Electronics. He worked as photolithography engineer for 2 years. And then he moved to DRAM development team. He served as project leader for 90nm, 60nm, 25nm, 20nm,1y DRAM development. His outstanding developments are 2.6Fx3.0F cell layout and honeycomb layout of cell capacitor for DRAM, which became standard feature in all DRAM makers. In 2021, he joined SKhynix, where he developed next generation technologies for Memory Devices. 3D DRAM structure and cell architecture developments. Hybrid wafer bonding for memory device. IGZO transistor & product, HfO thin film application for next generation DRAM, NAND.

- 1995, Ph.D. Material Science KAIST, "MOCVD YBCO superconducting thin film"
- 1995~2019, Samsung Electronics, Semiconductor R&D center.

: Photolithography – i-line, KrF, ArF lithography & OPC
: DRAM Product - 140nm, 90nm, 60nm, 25nm, 20nm, D1y
: NAND Product - 20nm planar NAND

- 2021~2022, SK Hynix, R&D Center for Future Technology

: Next Generation DRAM, 3D DRAM development
: Hybrid wafer bonding for memory device
: IGZO transistor & product, HfO DRAM, NAND

- Others

: 1999~2000, Post Doctor, UC Berkeley EECS, EUV mask & process.
: 2019~2020, OSAKA university, ISIR invited professor
: Papers 20+ (Journal, VLSI), Patents 35+ (US patent)